AMENDMENTS TO THE CLAIMS

Claim 1 (currently amended): A data transfer interface, comprising:

a first receiver and driver pair coupled to a first segment of a first data bus, said first receiver and driver pair being configured to receive data on said first segment using said first receiver and selectively place data on said first segment using said first driver;

a second receiver and driver pair coupled to a second segment of said first data bus, said second receiver and driver pair being configured to receive data on said second segment using said second receiver and selectively place data on said second segment using said second driver; and

a selector circuit connected to said first and second receiver and driver pairs, said selector circuit selectively operating said first and second receiver and driver pairs according to a state of a command/address bus coupled to said selector circuit ~~a selection signal~~ such that in a first state of said command/address bus ~~operating mode~~ said first receiver and driver pair passes data between said first bus segment and an I/O device and bypasses said second bus segment, and in a second state of said command/address bus ~~operating mode~~ said first and second receiver and driver pairs pass data between respective adjacent bus segments and bypass said I/O device.[[;]]

~~wherein said first and second receiver and driver pairs and said selector circuit are disposed on a same integrated circuit.~~

wherein said first and second segments of said first data bus is of a first data width and said I/O device is of a second data width, said first and second data widths being unequal.

Claims 2-6 (canceled):

Claim 7 (original): An interface as in claim 1, wherein said I/O device comprises a memory device.

Claim 8 (original): An interface as in claim 1, wherein said I/O device comprises a second data bus.

Claim 9 (currently amended): A data transfer interface, comprising:

a first receiver and driver pair coupled to a first segment of a first data bus, said first receiver and driver pair being connected to receive data on said first segment using said first receiver and selectively place data on said first segment using said first driver;

a second receiver and driver pair coupled to a second segment of said first data bus, said second receiver and driver pair being connected to receive data on said second segment using said second receiver and selectively place data on said second segment using said second driver;

a second data bus;

a device, coupled to said second data bus; and

an interface circuit coupled to a command/address bus, said first and second receiver and driver pairs, and said second data bus;

wherein

said interface circuit is configured, based on a state of said command/address bus, to receive data from said first receiver and selectively place said data for said device on said second data bus and receive data on said second data bus and selectively place said data on said first data bus, and

~~said first and second receiver and driver pairs, said second data bus, and said device are located on a same integrated circuit.~~

said first and second segments of said first data bus is of a first data width and said second data bus is of a second data width, said first and second data widths being unequal.

Claim 10-14 (canceled):

Claim 15 (original): The interface of claim 9, wherein said first receiver and driver pair is coupled to said first segment via a first set of I/O pins, and said second receiver and driver pair is coupled to said second segment via a second set of I/O pins.

Claim 16 (original): The interface of claim 9, wherein said interface circuit further comprises at least one of a multiplexer and demultiplexer that performs a data rate conversion between said first and second data buses.

Claim 17 (original): The interface of claim 9, wherein said interface circuit further comprises a multiplexer and a demultiplexer which perform data rate conversions for data received on said first data bus that is placed on said second data bus and for data received on said second data bus that is placed on said first data bus.

Claim 18 (original): The interface of claim 9, wherein said interface circuit further comprises at least one of a coder and decoder that performs at least one of a data encoding and decoding conversion between said first and second data buses.

Claim 19 (original): The interface of claim 9, wherein said interface circuit further comprises a voltage converter that performs a voltage level conversion between said first and second data buses.

Claim 20 (canceled):

Claim 21 (original): The interface of claim 9, wherein said second data bus is connected to at least one memory device.

Claim 22 (original): The interface of claim 9, wherein said first data bus is connected to a memory controller.

Claim 23 (original): The interface of claim 9, wherein said first data bus is connected to a processor.

Claim 24 (original): The interface of claim 9, wherein said first data bus operates at a first data rate faster than a second data rate at which said second data bus operates.

Claim 25 (original): The interface of claim 9, wherein said first data bus operates at a first voltage level less than a second voltage level at which said second data bus operates.

Claim 26 (original): The interface of claim 9, wherein said first data bus transmits analog signals.

Claim 27 (original): The interface of claim 9, wherein said first data bus transmits digital signals.

Claim 28 (original): The interface of claim 9, wherein said first data bus transmits radio-frequency (RF) signals.

Claim 29 (canceled):

Claim 30 (original): The interface of claim 9, wherein said first data bus is a substantially stubless data bus.

Claim 31 (currently amended): A memory module, comprising:

at least one memory device, each one of said at least one memory device being disposed on an integrated circuit, and comprising:

a memory; and

a data transfer interface connected to a first data bus and to said at least one memory device by a second data bus, said data transfer interface comprising:

a first receiver and driver pair coupled to a first segment of a first data bus, said first receiver and driver pair being connected to receive data on said first segment using said first receiver and selectively place data on said first segment using said first driver;

a second receiver and driver pair coupled to a second segment of said first data bus, said second receiver and driver pair being connected to receive data on said second segment using said second receiver and selectively place data on said second segment using said second driver; and

an interface circuit coupled to a command/address bus, said first and second receiver and driver pairs and a second data bus, wherein said interface circuit is configured, based on a state of said command/address bus, to receive data from said first receiver and selectively place said data for the memory on said second data bus, and receive data from the memory on said second data bus and selectively place said data on said first data bus;

wherein

said first and second segments of said first data bus is of a first data width and said second data bus is of a second data width, said first and second data widths being unequal; and

said second bus is coupled to said memory.

Claim 32-36 (cancel):

Claim 37 (original): The memory module of claim 31, wherein said first receiver and driver pair is coupled to said first segment via a first set of I/O pins, and said second receiver and driver pair is coupled to said second segment via a second set of I/O pins.

Claim 38 (original): The memory module of claim 31, wherein said interface circuit further comprises at least one of a multiplexer and demultiplexer that performs a data rate conversion between said first and second data buses.

Claim 39 (original): The memory module of claim 31, wherein said interface circuit further comprises a multiplexer and a demultiplexer which perform data rate conversions for data received on said first data bus that is placed on said second data bus and for data received on said second data bus that is placed on said first data bus.

Claim 40 (original): The memory module of claim 31, wherein said interface circuit further comprises at least one of a coder and decoder that performs at least one of a data encoding and decoding conversion between said first and second data buses.

Claim 41 (original): The memory module of claim 31, wherein said interface circuit further comprises a voltage converter that performs a voltage level conversion between said first and second data buses.

Claim 42 (original): The memory module of claim 31, wherein said first bus includes a first number of data paths and said second bus includes a second number of data paths, and said first number of data paths is less than said second number of data paths.

Claim 43 (original): The memory module of claim 31, wherein said second data bus is connected to at least one memory device.

Claim 44 (original): The memory module of claim 31, wherein said first data bus is connected to a memory controller.

Claim 45 (original): The memory module of claim 31, wherein said first data bus is connected to a processor.

Claim 46 (original): The memory module of claim 31, wherein said first data bus operates at a first data rate faster than a second data rate at which said second data bus operates.

Claim 47 (original): The memory module of claim 31, wherein said first data bus operates at a first voltage level less than a second voltage level at which said second data bus operates.

Claim 48 (original): The memory module of claim 31, wherein said first data bus transmits analog signals.

Claim 49 (original): The memory module of claim 31, wherein said first data bus transmits digital signals.

Claim 50 (original): The memory module of claim 31, wherein said first data bus transmits radio-frequency (RF) signals.

Claim 51 (canceled):

Claim 52 (original): The memory module of claim 31, wherein said first data bus is a substantially stubless data bus.

Claim 53 (currently amended): A data exchange system, comprising:

a first data bus having at least first and second bus segments;

a controller connected to place data on and receive data from said first data bus;

a processor coupled to said controller, and

a data transfer interface, disposed on an integrated circuit and comprising:

a first receiver and driver pair coupled to a first segment of a first data bus, said first receiver and driver pair being connected to receive data on said first

segment using said first receiver and selectively place data on said first segment using said first driver;

a second receiver and driver pair coupled to a second segment of said first data bus, said second receiver and driver pair being connected to receive data on said second segment using said second receiver and selectively place data on said second segment using said second driver;

a second data bus;

a device, coupled to the second data bus; and

an interface circuit coupled to a command/address bus, said first and second receiver and driver pairs and a second data bus, wherein said interface circuit is configured, based on a state of said command/address bus, to receive data for the device on said first data bus and selectively place said data on said second data bus, and receive data from the device on said second data bus and selectively place said data on said first data bus;[[.]]

wherein said first data bus is of a first data width, said second data bus is of a second data width, said first and second data widths being unequal.

Claims 54 - 56 (cancel):

Claim 57 (previously presented): A method of data communication comprising:

receiving data at first and second receivers coupled to respective first and second segments of a first data bus;

driving data using first and second drivers coupled to said respective first and second segments, said driving being performed according to a state of a command/address bus ~~a selection signal,~~ such that when said command/address bus is in a first state ~~in a first operating mode~~ a first receiver and driver pair passes signals between said first segment of said first data bus and an I/O device and bypass said second segment, and when said command/address bus is in a second state ~~in a second operating mode~~ said first and a second receiver and driver pairs pass signals between respective adjacent bus segments and bypass said I/O device;

wherein said first data bus is of a first data width, said I/O device is of a second data width, said first and second data widths being unequal. ~~said first and second receivers, said first and second drivers, and said I/O device are disposed on a same integrated circuit.~~

Claim 58 (original): A method as in claim 57, wherein said I/O device comprises a memory device.

Claim 59 (original): A method as in claim 57, wherein said I/O device comprises a second data bus.

Claim 60 (currently amended): A method of data communication, comprising:

connecting an interface circuit having first and second receiver and driver pairs to respective first and second segments of a first data bus that operates at a first data rate;

connecting said interface circuit to at least one device on a second data bus that operates at a second data rate;

receiving and transmitting data on said first data bus using said first and second receiver and driver pairs;

receiving and transmitting data on said second data bus; and

based on a state of an command/address bus coupled to said interface circuit,

selectively placing data received from said first bus segment on said second bus segment[[;]] when said command/address bus is in a first state;

selectively placing data received from said second bus segment on said first bus segment[[;]] when said command/address bus is in a second state; and

selectively converting data received from one of said first and second data buses for use on the other of said first and second data buses;

wherein said first data bus is of a first data width, said second data bus is of a second data width, said first and second data widths being different. ~~said interface circuit, said second data bus, and said at least one device are disposed on a same integrated circuit.~~

Claim 61-65 (canceled):

Claim 66 (original): A method as in claim 60, wherein said first data rate is faster than said second data rate.

Claim 67 (original): A method as in claim 60, further comprising converting received data between said first data rate of said first data bus and said second data rate of said second data bus.

Claim 68 (original): A method as in claim 60, further comprising converting received data between a first encoding of said first data bus and a second encoding of said second data bus.

Claim 69 (original): A method as in claim 60, further comprising converting received data between a first voltage level of said first data bus to a second voltage level of said second data bus.

Claim 70 (original): A method as in claim 69, wherein said first voltage level is less than said second voltage level.

Claims 71-72 (canceled):

Claim 73 (original): A method as in claim 60, wherein devices of a first technology communicate with said interface circuit using said first data bus and devices of a second technology communicate with said interface circuit using said second data bus.

Claim 74 (original): A method as in claim 73, wherein said devices of said first technology include at least one processor.

Claim 75 (original): A method as in claim 73, wherein said devices of said second technology include at least one memory device.

Claim 76 (canceled):

Claim 77 (original): A method as in claim 60, wherein said first data bus is a substantially stubless data bus.